

<b>Notice of References Cited</b>	Application/Control No. 09/927,204	Applicant(s)/Patent Under Reexamination FOLTIN ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

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	B	US-6,453,436	09-2002	Rizzolo et al.	714/726
	C	US-6,158,022	12-2000	Avidan, Jacob	714/33
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**NON-PATENT DOCUMENTS**

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	U	Kulshreshtha et al., "Transistor-level Timing Analysis using Embedded Simulation" IEEE 2000 pg. 344-349.
	V	Albrecht et al., " Cycle Time and Slack Optimization for VLSI-chips" pg.232-238 1999 IEEE/ACM International Conference on Computer-aided Design
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.